Code No.: **40403/30403** **MR14/MR13**

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad

II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019

Subject: **Switching Theory and Logic Design**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer **ALL** questions of the following **5x1Mark=5 Marks**

1. Find the 9's complement of the number 143.
2. Draw the 3-variable k-map with minterms.
3. Write the characteristic equation for D Flip-Flop.
4. State variable modulus counter?
5. What is ASM?

II. Answer **ALL** questions of the following **10x2Marks=20 Marks**

1. State about logic design and what do you mean by positive logic system?
2. State the Duality Theorem.
3. Draw the sum output of half adder using only NOR gates.
4. Realize Full adder using two half adders and logic gates.
5. Write a short note on master slave J-K flip-flop
6. Draw the k-map for next state of D-Flip flop
7. Draw the logic diagram of a 2-bit ring counter.
8. How states are reduced in sequential circuit design?
9. Mention the limitations of FSM.
10. Why does merger chart is require?

PART-B

Answer **ALL** questions of the following **5x10 Marks= 50Marks**

1. Write the theorems and postulates of Boolean algebra.

(OR)

2. a) Develop a Gray code for $(84)_{10}$ and $(35)_{10}$ and convert the same to Hex sequence [6M]
   b) Explain different error detecting codes [4M]
3. Obtain the simplified expressions in (1) sum of products and (2) product of sums X'Z'+Y'Z'+YZ'+XYZ

(OR)

4. Define prime implicant and EPI. Minimize the
   f(A,B,C,D,E) = ∑M(0,1,2,3,4,6,9,10,15,16,17,18,19,20, 23, 25, 26, 31)by tabular method
5. a) Implement edge triggered D flip flop with SR latch explain with truth table?
   b) Convert D flip flop in to JK flip flop?

(OR)

6. Realize SR latch using only a) NOR gates and b) NAND gates. Also draw the truth tables.
7. a) Design 4 bit serial in serial out shift register using D flip flops ?
   b) Design mode 4 bit ring counter using JK flip Flops?

(OR)

8. Draw the logic diagram of a 4-bit serial input and parallel output shift register. Explain the operation with the help of timing diagrams.
9. a) Explain in detail the block diagram of ASM chart.
   b) Draw an ASM chart to convert D-flip flop to T-flip flop.

(OR)

10. Explain the following: Merger chart and Minimal cover table.

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MR14

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019

Subject: **Electronic Circuits**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer **ALL** questions of the following **5x1Mark=5 Marks**

1. What are the different configurations of BJT?
2. What are the advantages of push pull amplifiers?
3. Write condition for oscillations
4. Define low pass filter.
5. What are the applications of bistable multivibrator?

II. Answer **ALL** questions of the following **10x2Marks=20 Marks**

1. Give the differences between voltage amplifier and power amplifier.
2. Draw the small signal model for a common source FET amplifier.
3. Classify large signal amplifiers based on its operating point
4. Derive the efficiency of class B power amplifier.
5. Discuss current shunt amplifier.
6. State the Barkhausen criterion for an oscillator.
7. Explain working of high pass RC circuit.
8. What is mean by positive clamping and negative clamping?
9. How many methods of triggering are there for multi vibrators? Name them.
10. Describe the behavior of transistor as a switch.

PART-B

Answer **ALL** questions of the following **5x10 Marks= 50Marks**

1. Explain with circuit diagram and relevant expressions working of common gate FET model.

OR

2. a) Design the circuit diagram of CS amplifier. With the help of small signal model, derive the expressions for input impedance, output impedance and voltage gain.
   b) The h-parameters of CE amplifier with Rs= 1 k , RL=10k , hie=1.1 K, hre = 2.5 x 10^{-4} , hfe=50 and hoe-24 μA/V. Find out current and voltage gains with and without source resistance, input and output impedances?
3. a) Explain working of Crystal oscillator
   b) Design a phase shift oscillator using an FET having g_m = 4500 μS, r_d = 45 kΩ, and a feedback circuit value of R = 12 kΩ.Select the value of C for oscillator operation at 6 kHz and R_D for A >27 to ensure oscillator action.

OR

4. a) Write short notes on requirement and types of heat sinks for power dissipation in large signal amplifiers.
   b) With the help of an neat circuit diagram, explain the operation of a complementary symmetry configured class B power amplifier.

5. a) Explain voltage shunt feedback amplifiers &current series feedback amplifiers.
   b) The gain of an amplifier is decreased to 1000 with negative feedback from its gain of 5000. Calculate the feedback factor and amount of negative feedback in dB.

OR

6. a) Draw the circuit diagram and explain the working principle of Hartley oscillator. Also derive the expression for frequency of oscillation and condition for oscillations.
   b) In an RC phase shift oscillator, if the frequency of oscillation is 955 Hz and $R_1 = R_2 = R_3 =$ 680 kΩ Find the value of capacitors.
7. a) Derive an expression for the output of a low pass circuit excited by an step input.
   b) A 100 Hz square wave with peak to peak amplitude of 9V is applied to a differentiating circuit with R=1MΩ and C= 100pF. Calculate and sketch the waveform of the output

OR

8. a) With the help of neat circuit diagram explain the working of negative clamping circuit. What is the effect of Rs and R_f on clamping circuit output.
   b) Design a diode clamper to restore the positive peaks of 1kHz input signal to a voltage level equal to 5V. Assume the voltage drop across diode is 0.7 V.
9. a) With the help of neat circuit diagram and waveforms explain the working of Schmitt trigger
   b) Find the period of output and frequency of oscillation of an astable multivibrator with R1=R2=25KΩ and C1=C2=0.2μF

OR

10. a) Write short notes on commutating capacitors. What are the other names of commutating capacitors?
    b) Explain the working principle of mono stable multivibrator and derive an expression for its pulse width.

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MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019

Subject: **Network Theory**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

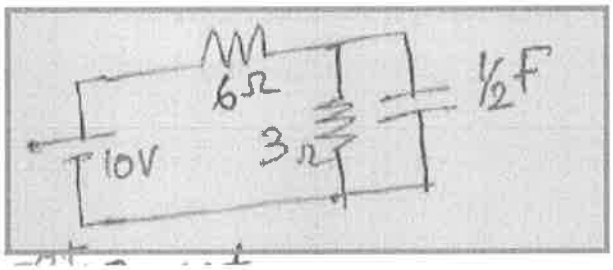
PART – A

I. Answer **ALL** questions of the following **5x1Mark=5 Marks**

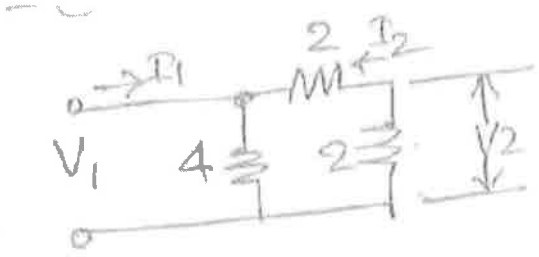
1. The Voltage from phase 'a' to neutral 'n' in balanced three phase circuit is $230\angle 30^0$ volts. If the phase sequence is a-b-c what is values of V_{ab}.
2. A Voltage impulse of $\delta(t)$ is forced through an indicator L. Find the current i(t) through the indicator.
3. What is immittance
4. What is the condition for reciprocity 'In' ABCD parameter network.
5. Define even symmetry in Fourier analysis.

II. Answer **ALL** questions of the following **10x2Marks=20 Marks**

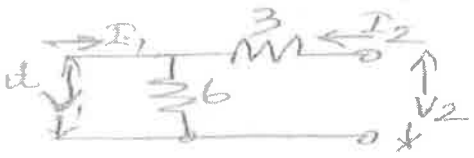
1. In a two wattmeter method to measure the power the wattmeter readings are 2000 and 1500 watts, respectively. The supply is 440V, 3ϕ, 50 Hz and load is balanced and delta connected. Find the impedance in each phase.
2. A balanced connected load of (2+j3) ohms per phase is connected in a balanced 3-phase, 440V supply. The phase current is 10A. Find i) Total active power ii) Reactive power.
3. The current in a R-L series circuit is given as $i(t) = -5e^{-10t}$. Find i) Time constant ii) initial rate of change of current.
4. Find the time constant for given circuit



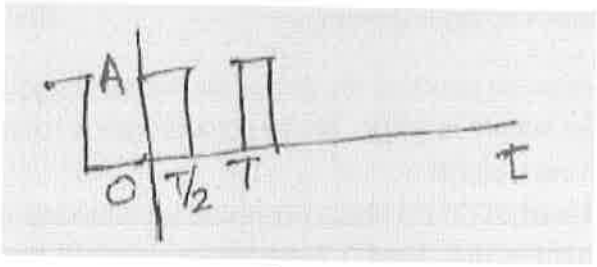
5. Obtain pole & zero locations for $f(t) = \acute{e}^{\sigma t}\cos\omega t$.
6. Find $\frac{V1}{V2}$ for given resistive circuit



7. Find 'Y' parameters for given circuit



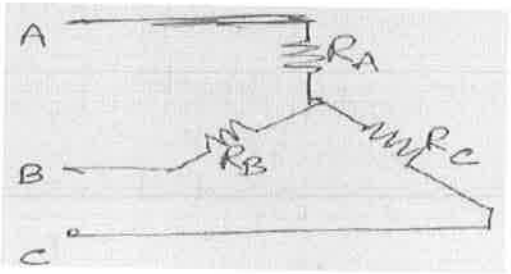
8. The following euations represent a two-port network $V_1 = 5\ I_1 + 2\ I_2$ $V_2 = 2\ I_1 + I_2$ A load of 3Ω is connected across port 2. Calculate Z_{in}
9. Define Neper. Express 10 dB attenuation in nepers.
10. The periodic wave shown in fig is applied across one ohm resistor. Find the power absorbed by resistor.



PART-B

Answer **ALL** questions of the following **5x10 Marks= 50Marks**

1. a) Consider a star network shown in fig. The resistance between terminals A & B with 'C' open is 6Ω. The resistance between B&C with 'A' open is 11Ω. The resistance between C&A with 'B' open is 9Ω. Find R_A,R_B,R_C



b) A 3ϕ load has a resistance of 10 Ω in each phase and is connected in i) star ii) delta against the power supply of 400V, 3ϕ supply. Compare the power consumed in both cases.

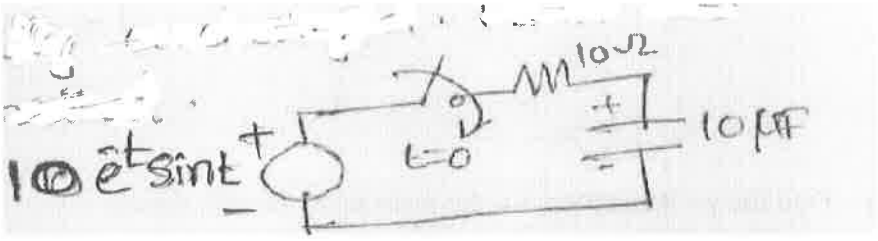
OR

2. a) Three identical impedance of (3+j4) Ω are connected in delta. Find an equivalent star network such that the line current is same when connected to same supply.

b) A balanced star connected load is supplied from symmetrical 3ϕ, 400V system. The current in each phase is 30A and lags behind the phase voltage. Find total power and draw the phasor diagram.

3. a) A dc voltage of 200V suddenly applied to a series RL circuit R=20Ω and L=0.2H. Find voltage drop across inductor at the instant of switching and .02 sec later.

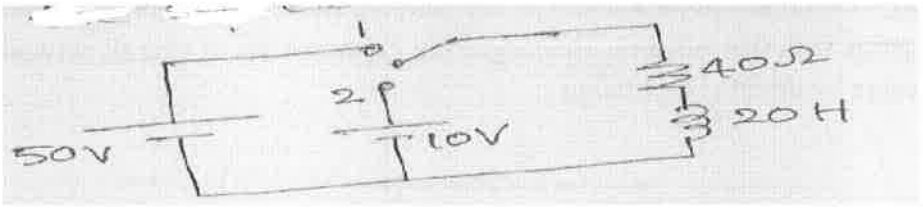
   b) In the circuit shown the switch is closed at t=0. The capacitor is initially uncharged. Find i(t) by laplace transform method.



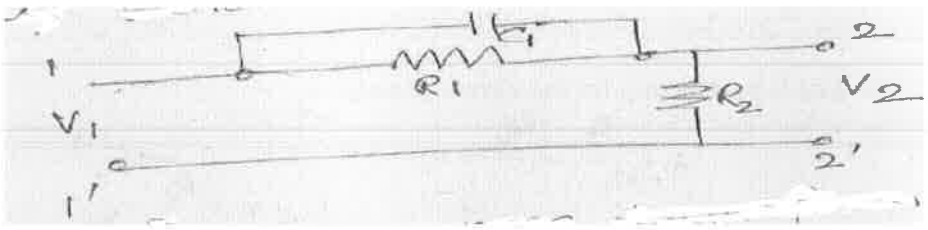
OR

4. a) A resistance R and 5μF capacitor are connected in series across at 100V de supply. Calculate the value of 'R' such that the voltage across capacitor becomes 50V in 5 sec after circuit is switched on.

   b) In the circuit shown in fig switch is in position 1 for a long time and moved to position 2 at t=0. Find the expression for i(t).



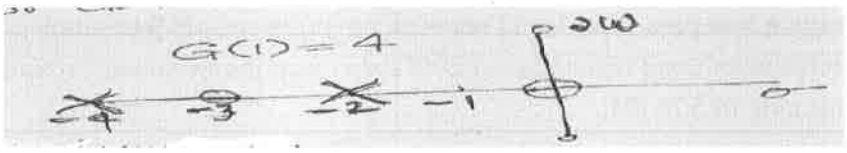
5. a) Obtain the $G_{12}(S)$ for the two-port network.



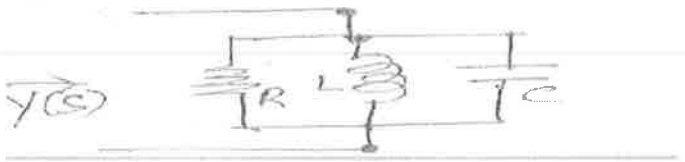
   b) Find the inverse transform of the function $V(S) = \frac{2}{S^3+12S^2+36S}$

OR

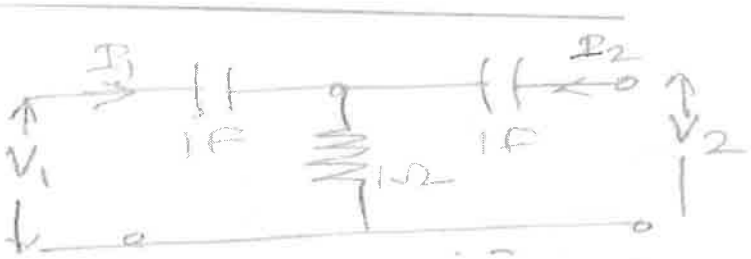
6. a) The pole-zero constellation is shown in fig obtain expression for gain that is ratio of polynomial in 'S'.



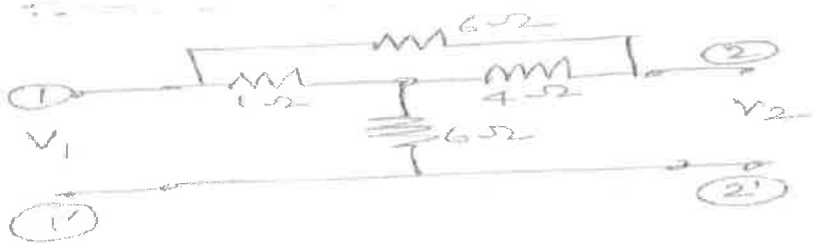
   b) Find admittance function for the network shown.



7. a) Find the transmission parameters for given network.

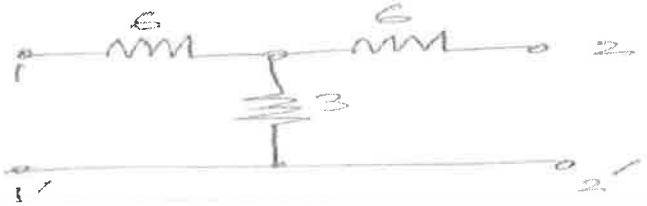


b) Find the γ - Parameters for the resistance network shown

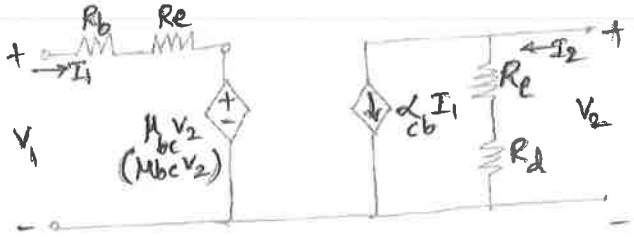


OR

8. a) Determine Z-parameters of the network shown. An identical network is connected in series with this network. Determine the Z-parameters of overall network & verify the same by direct computation



b) Calculate h-parameters for the circuit shown



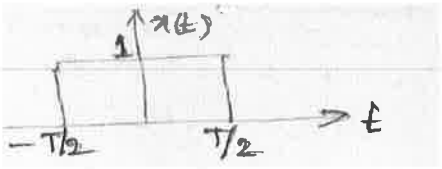
9. a) Calculate for a LPF 'T' network i) Characteristic impedance ii) cut=off frequencies given $Z_1=\frac{1}{j\omega c}$ and $Z_2= j\omega L$

b) Design a low pass filter for Π network having a cut-off frequency of 1 kHz to operate with a terminated load resistance of 200Ω also find the frequency at which the filter offers attenuation of 17.372 dB.

OR

10. a) Explain about DIRICHLET conditions.

b) Find the Fourier transform of the gate function shown in fig.



Code No.: **40206** **MR14**

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019

Subject: **Electrical Machines -II**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer **ALL** questions of the following **5x1Mark=5 Marks**

1. Define voltage transformation ratio of a transformer.
2. What advantage has the star connection over the delta connection of transformer
3. Why is the rotor rheostat starter unsuited for a cage motor?
4. What is the advantage of using a capacitor – start motor over a resistance – start spilt phase motor
5. What is the condition for maximum torque at starting in a 3-ϕ induction motor?

II. Answer **ALL** questions of the following **10x2Marks=20 Marks**

1. What is a transformer? Differentiate step up and step down transformers?
2. Draw the equivalent circuit of a transformer.
3. Why tertiary winding is used in transformers?
4. Why tapping are on H.V side in top changing transformer?
5. What are the various types of starters used for squirrel cage motors?
6. Define the term slip of the induction motor.
7. Explain the effect of slip on the rotor frequency.
8. How the speed is controlled by adding an external resistance in the rotor circuit?
9. Why are centrifugal switches provided on many single phase induction motors?
10. What is split phase motor?

PART-B

Answer **ALL** questions of the following **5x10 Marks= 50Marks**

1. Explain the principle of working of a single phase transformer

OR

2. A 300kVA, 11000/440V, single phase, 50Hz, transformer gave the following test results
   O.C test: (L.V side) : 440V, 21.1amp, 1.3kw; S.C test ; (H.V side) : 600V, 15 amp, 2.8kw;
   Calculate efficiency and regulation for full load at 0.8P.f lagging.
3. With the help of phasor diagram explain how two phase supply can be obtained from three phase supply using Scott connection.

OR

4. A three phase, 100kVA, 6600/1100V transformer is delta connected on the primary and star connected on the secondary. The primary resistance per phase is 1.8Ω and secondary resistance per phase is 0.025Ω; determine the efficiency when the secondary is supplying full load at 0.8P.f and the iron loss is 15kw.
5. Develop an equivalent circuit for three phase induction motor state the difference between exact and approximate equivalent circuit.

OR

6. Derive the relation between rotor output, rotor input and slip in case of three phase induction motor.
7. A 20hp, 400V, 50Hz, three phase induction motor which is star connected has the following test data: No load test : 400V, 9A, cosϕ=0.2 Blocked rotor test : 200V, 50A, cosϕ=0.4
   Draw a circle diagram and determine: i) line current ii) power factor iii)slip iv)efficiency

OR

8. Explain the induction generator principle with its phasor diagram.
9. Derive equivalent circuit of a single phase induction motor with the help of double field revolving theory.

OR

10. Explain the operation of single phase induction motor using split phase technique.